An Algorithm for Designing Upper-Delay Bounded Switched Local Area Networks

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Abstract
The designs of switched Local Area Networks (switched LANs) in practice are usually based on heuristics and experience; in fact, in many cases, no network design is carried out, but only network installation (network cabling and nodes/equipment placements). This may have been as a result of the absence of generally known methods for designing such networks. Also, there is the need for deterministic guarantees on delays when designing switched LANs, as it has been generally agreed that these delays are useful engineering quantities. This is because, if the maximum delay between two nodes of a network is unknown, it is impossible to provide a deterministic guarantee of worst case response times of packets " flows in the network. This paper reports the development of an algorithm for designing upper-delay bounded switched LANs.

Keywords: Upper-Bounded End-To-End Delay, Switched Local Area Networks

1.IntroductionThere has been a strong trend away from shared medium (in the most recent case, the use of Ethernet hubs) in Ethernet Local Area Networks (LANs) in favor of switched Ethernet LANs installations [1, p.102]. But LANs " designs in practice are based on heuristics and experience. In fact in many cases, no network design is carried out, but only network installation (network cabling and nodes/equipment placements) [2], [3]. But there is the need for deterministic guarantees on delays when designing switched LANs; because these delays are useful engineering quantities [4]. This is as a result of the fact that, if the maximum delay between two nodes of a network is unknown, it is impossible to provide a deterministic guarantee of worst case response times of packets " flows in the network [5].

Network issues of concern to this research work are, therefore, network end-to-end delays and the capability of a network to transfer a required amount of information in a specified time. Network switches cannot just be placed and installed in a switched LAN without any formalism for appropriately specifying the switches, as the speed of a network is limited by the electronic processing at the nodes of the network [6, p.339], [7, p.49]. How, therefore, should appropriate number of switches, and the capacities of the switches for any switched LAN be determined? Network hosts cannot also continue to be added to a network indiscriminately; as end-to-end delay depends on the time of day, and at certain times of the day, more users are logged on to the network, leading to an increase in end-to-end delays [8], [9, p.876]. We have reported in [10], the development of a maximum delay packet switch model and in [11] it was shown that it is not correct to enumerate the end-to-end delays of a switched LAN in terms of the hosts that are connected to the network; but that this enumeration should be done in terms of the switches. In this paper, we describe the development of an algorithm for designing upper-delay bounded switched LANs.

2.Switched Local Area Networks and End-To-End Delays

A Switched LAN is a LAN that uses switches to connect individual nodes or segments. On switched networks where nodes are directly connected to switches with full-duplex links, the communication is point-to-point. That is, a switched LAN isolates network traffic between sending and receiving nodes. In this configuration, switches break up collision domains into small groups of devices, effectively reducing the number of collisions [12], [13]. Furthermore, with micro-segmentation with full-duplex links, each device is isolated in its own segment in full duplex mode and has the entire port throughput for its own use; collisions are therefore, eliminated [14]. The CSMA/CD (Carrier Sense Multiple Access with Collision Detection protocol does not therefore, play any role in switched networks [1, p.102].

Delay is the elapsed time for a packet to be passed from the sender through the network to the receiver [15]. The concept of end-to-end is used as a relative comparison with hop-by-hop, as data transmission seldom occurs only between two adjacent nodes, but via a path which may include many intermediate nodes. End-to-End delay is the delay required to deliver a packet from a source to destination [8].

The path transversed by a packet through a network can be modeled as a sequence of queuing systems [3], [16, p.539]; this is illustrated in Figure 1. The dashed arrows show packets from other flows that may 'interfere' with the packet of interest in the sense of contending for buffers and transmission along the path. The performance experienced by a packet along the path is the accumulation of the performance experienced along the N queuing systems; for example, the total end-to-end delay is the sum of the individual delays experienced at each system [16, p.539]. If we can guarantee that the delay at each system can be kept below some upper bound, then the end-to-end delay can be kept below the sum of the upper bounds [16, p.540]. It is therefore easy to see that, using our maximum packet delay model for an N-port packet switch (reported in [10]), we can calculate the maximum end-to-end delay of a packet from origin to destination if we know the number of switches on its route from origin to destination. If we know all the end-to-end delays of a switched LAN, the maximum delay constraint of the applications to be deployed in the network, we would then be able to calculate all the maximum end-to-end delays of the switched LAN and ensure that all the maximum end-to-end delays are less than the maximum delay constraint of the applications to be deployed in the network.

This upper-delay bounded switched LAN design approach finds support with the view of Metzler in [17] that 'the latency of any network has a major impact on the applications that can be deployed in the network'. Moreover, Georges, Divoux and Rondeau stated in [13] with respect to switched Ethernet networks in an industrial environment that, the network calculus is used to determine the upper-bounded end-to-end delay of each packet; and that, if all the end-to-end delays are less than the time-cycle of the programmable controllers, then the network organization (switches' placements) is in accordance with the application constraint.

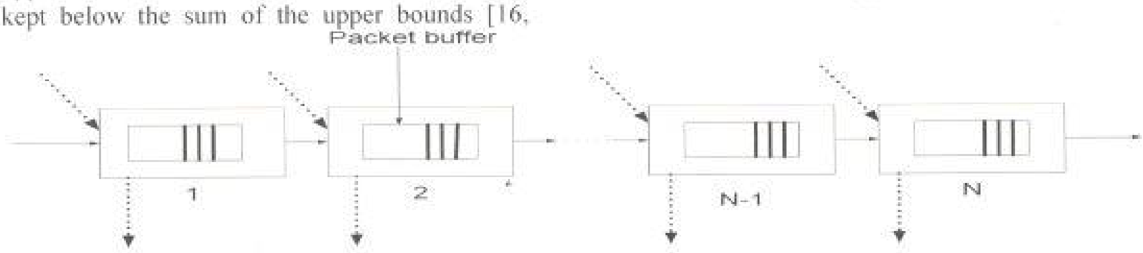

Figure 1 The end-to-end QoS of a packet switch along a line transversing N queuing systems. Source: [16, p.539]

3. Development of Switched Local Area Network Design Algorithm

Consider Figure 2. Let us assume that switches S_1, S_2, S_3,…,S_8 will be placed by the network designer (installer) as a result of the number of hosts and the locations of the hosts in a new LAN installation. We have been able to deduce that, if;

m = the number of switches in the LAN,

p = the number of maximum end-to-end delays required for the design of an upper delay bounded switched LAN,

then $$p = \sum_{x=0}^{m-1}(m-x) \qquad (1)$$

Here, m = 8, $p = \sum_{x=0}^{8-1}(8-x) = 36$ maximum end-to-end delays.

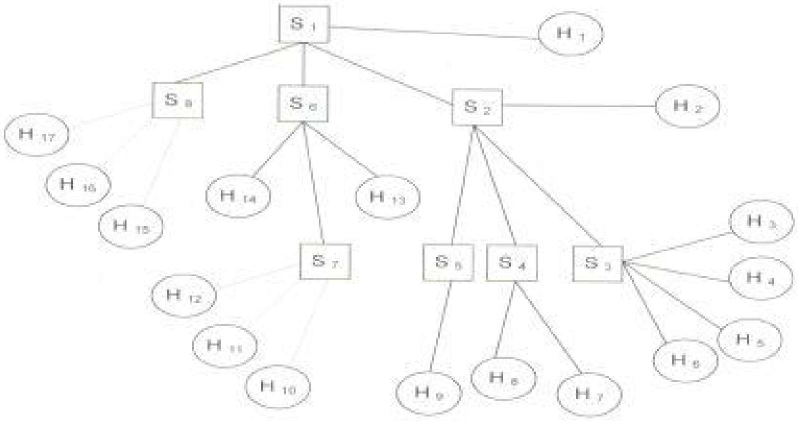

Figure 2 An hypothetical Switched LAN having 8 switches (Si's) and 17 hosts (Hi's)

We use Figure 2 to illustrate how to enumerate the maximum end-to-end delays for any switched LAN. Our method (algorithm) for this enumeration which we call, 'right-most, pre-order transversal' has two steps:
Process the root switch,
Transverse the right-most, sub-tree pre-order, until all the switches have been processed.
Performing 'left-most, pre-order transversal' (the opposite of 'right-most, pre-order transversal') results in the same solution. The important thing is that, both methods cannot be mixed for the same LAN design process.

Using the right-most, pre-order transversal, the required end-to-end delays are enumerated as follows (we take switch S_1 as the root switch).

1. Switch S_1 is placed.
2. Next, place switch S_2 and connect S_1 to S_2.

Now, for any host that is attached to switch S_1 to communicate with any host that is attached to switch S_2, data packets will experience delay in switch S_1 and switch S_2 and vice versa; this is 1 end-to-end delay.
(delay in S_1 + delay in S_2) = 1 end-to-end delay

3. Next, place switch S_3 and connect to switch S_2.

Again, for any host that is attached to switch S_1 to communicate with any host that is attached to switch S_3, the data packets will experience delays in switch S_1, switch S_2, and switch S_3; this is 1 end-to-end delay.
(delay in S_1 + delay in S_2 + delay in S_3) = 1 end-to-end delay
Also, for any host that is attached to switch S_2 to communicate with any host that is attached to switch S_3, the data packets will experience delays in switch S_2 and switch S_3; this is one end-to-end delay.
(delay in S_2 + delay in S_3) = 1 end-to-end delay

We now have 3 end-to-end delays already. This enumeration procedure is continued by placing switches 4, 5, 6, 7, and 8 in that order. It can also be seen that, for any host that is attached to switch S_1 to communicate with another host that is attached to the same switch S_1, data packets will experience delay only in switch S_1; this is 1 end-to-end delay. We have a similar situation if any host that is attached to switch S_2 wants to communicate with another host that is attached to the same switch S_2. This is similarly the case with hosts that are attached to switches 3, 4,….8 respectively. These eight situations give us 8 end-to-end delays. We now explain the enumeration of all the end-to-end (maximum end-to-end) delays of the switched LAN.

Assuming that, the maximum time for any packet to cross $S_i = x_i$ seconds, $i = 1, 2, \ldots, m$, then, associated with each of the switches S_1, S_2, S_3, S_4, S_5, S_6, S_7, and S_8, is a maximum end-to-end delay of x_1 seconds, x_2 seconds, x_3 seconds, x_4 seconds, x_5 seconds, x_6 seconds, x_7 seconds, and x_8 seconds respectively. We now list all the other maximum end-to-end delays as each switch is being placed.

When S_2 is placed, the maximum end-to-end delay is:

$$x_2 + x_1$$

When S_3 is placed, the maximum end-to-end delays are:

$$x_3 + x_2; x_3 + x_2 + x_1$$

When S_4 is placed, the maximum end-to-end delays are;

$x_4 + x_2$; $x_4 + x_2 + x_1$; $x_4 + x_2 + x_3$

When S_5 is placed, the maximum end-to-end delays are:

$x_5 + x_2$; $x_5 + x_2 + x_1$; $x_5 + x_2 + x_3$; $x_5 + x_2 + x_4$

When S_6 is placed, the maximum end-to-end delays are:

$x_6 + x_1$; $x_6 + x_1 + x_2$; $x_6 + x_1 + x_2 + x_3$; $x_6 + x_1 + x_2 + x_4$; $x_6 + x_1 + x_2 + x_5$

When S_7 is placed, the maximum end-to-end delays are:

$x_7 + x_6$; $x_7 + x_6 + x_1$; $x_7 + x_6 + x_1 + x_2$; $x_7 + x_6 + x_1 + x_2 + x_3$; $x_7 + x_6 + x_1 + x_2 + x_4$; $x_7 + x_6 + x_1 + x_2 + x_5$

When S_8 is placed, the maximum end-to-end delays are:

$x_8 + x_1$; $x_8 + x_1 + x_2$; $x_8 + x_1 + x_2 + x_3$; $x_8 + x_1 + x_2 + x_4$; $x_8 + x_1 + x_2 + x_5$

$x_8 + x_1 + x_6$; $x_8 + x_1 + x_6 + x_7$, where all the maximum end-to-end delays enumerated above are in seconds. Therefore, the following steps can be followed in attempts at automating the maximum end-to-end delays enumeration process.

STEP 1.

Place S_1

STEP 2.

Place S_2 and connect to S_1; additional end-to-end delays = 1 = no of switch already in the network. Switch already in the network is S_1. S_2 is attached to S_1. 1st maximum end-to-end delay is $x_2 + x_1$.

S_2 is the beginning switch AND S_1 is the ending switch OR S_2 is the ending switch AND S_1 is the beginning switch. The maximum end-to-end delay is: MAX. END-TO-END DELAY 1-2.

STEP 3.

Place S_3 and connect to S_2; additional end-to-end delays = 2 = no of switches already in the network. Switches already in the network are S_1 and S_2. S_3 is attached to S_2. 1st maximum end-to-end delay is $x_3 + x_2$. S_3 is the beginning switch AND S_2 is the ending switch OR S_3 is the ending switch AND S_2 is the beginning switch. The maximum end-to-end delay is: MAX. END-TO-END DELAY 2-3.

2nd maximum end-to-end delay is $x_3 + x_2 + x_1$; S_3 is the beginning switch AND S_1 is the ending switch OR S_3 is the ending switch AND S_1 is the beginning switch. Since S_3 is attached to S_2, the maximum end-to-end delay is: MAX END-TO-END DELAY 1-3 = MAX END-TO-END DELAY 3 + MAX END-TO-END DELAY 1-2.

STEP 4.

Place S_4 and connect to S_2; additional end-to-end delays = 3 = no of switches already in the network. Switches already in the network are; S_1, S_2, and S_3. S_4 is attached to S_2. 1st maximum end-to-end delay is $x_4 + x_2$. S_4 is the beginning switch AND S_2 is the ending switch OR S_4 is the ending switch AND S_2 is the beginning switch. The maximum end-to-end delay is: MAX. END-TO-END DELAY 2-4.

2nd maximum end-to-end delay is $x_4 + x_2 + x_1$; S_4 is the beginning switch AND S_1 is the ending switch OR S_4 is the ending switch AND S_1 is the beginning switch. Since S_4 is attached to S_2, the maximum end-to-end delay is: MAX END-TO-END DELAY 1-4 = MAX END-TO-END DELAY 4+ MAX END-TO-END DELAY 1-2.

3rd maximum end-to-end delay is $x_4 + x_2 + x_3$; S_4 is the beginning switch AND S_3 is the ending switch OR S_4 is the ending switch AND S_3 is the beginning switch. Since S_4 is attached to S_2, the maximum end-to-end delay is: MAX END-TO-END DELAY 3-4 = MAX END-TO-END DELAY 4 + MAX END-TO-END DELAY 3-2.

STEP 5.

Place S_5 and connect to S_2; additional end-to-end delays = 4 = no of switches already in the network. Switches already in the network are; S_1, S_2, S_3, and S_4. S_5 is attached to S_2. 1st maximum end-to-end delay is $x_5 + x_2$. S_5 is the beginning switch AND S_2 is the ending switch OR S_5 is the ending switch AND S_2 is the beginning switch. The maximum end-to-end delay is: MAX. END-TO-END DELAY 2-5.

2nd maximum end-to-end delay is $x_5 + x_2 + x_1$; S_5 is the beginning switch AND S_1 is the ending switch OR S_5 is the ending switch AND S_1 is the beginning switch. Since S_5 is attached to S_2, the maximum end-to-end delay is: MAX END-TO-END DELAY 1-5 = MAX END-TO-END DELAY 5 + MAX END-TO-END DELAY 1-2.

3rd maximum end-to-end delay is $x_5 + x_2 + x_3$; S_5 is the beginning switch AND S_3 is the ending switch OR S_5 is the ending switch AND S_3 is the beginning switch. Since S_5 is attached to S_2, the maximum end-to-end delay is: MAX END-TO-END DELAY 3-5 = MAX END-TO-END DELAY 5 + MAX END-TO-END DELAY 3-2.

4th maximum end-to-end delay is $x_5 + x_2 + x_4$; S_5 is the beginning switch AND S_4 is the ending switch OR S_5 is the ending switch AND S_4 is the beginning switch. Since S_5 is attached to S_2, the maximum end-to-end delay is: MAX END-TO-END DELAY 4-5 = MAX END-TO-END DELAY 5 + MAX END-TO-END DELAY 4-2.

STEP 6.

Place S_6 and connect to S_1; additional end-to-end delays = 5 = no of switches already in the network. Switches already in the network are; S_1, S_2, S_3, S_4, and S_5. S_6 is attached to S_1. 1st maximum end-to-end delay is $x_6 + x_1$. S_6 is the beginning switch AND S_1 is the ending switch OR S_6 is the ending switch AND S_1 is the beginning switch. The maximum end-to-end delay is: MAX. END-TO-END DELAY 1-6.

2nd maximum end-to-end delay is $x_6 + x_1 + x_2$. S_6 is the beginning switch AND S_2 is the ending switch OR S_6 is the ending switch AND S_2 is the beginning switch. Since S_6 is attached to S_1, the maximum end-to-end delay is: MAX END-TO-END DELAY 2-6 = MAX END-TO-END DELAY 6 + MAX END-TO-END DELAY 1-2.

3rd maximum end-to-end delay is $x_6 + x_1 + x_2 + x_3$; S_6 is the beginning switch AND S_3 is the ending switch OR S_6 is the ending switch AND S_3 is the beginning switch. Since S_6 is attached to S_1, the maximum end-to-end delay is: MAX END-TO-END DELAY 3-6 = MAX END-TO-END DELAY 6 + MAX END-TO-END DELAY 1-3.

4th maximum end-to-end delay is $x_6 + x_1 + x_2 + x_4$; S_6 is the beginning switch AND S_4 is the ending switch OR S_6 is the ending switch AND S_4 is the beginning switch. Since S_6 is attached to S_1, the maximum end-to-end delay is: MAX END-TO-END DELAY 4-6 = MAX END-TO-END DELAY 6 + MAX END-TO-END DELAY 1-4.

5th maximum end-to-end delay is $x_6 + x_1 + x_2 + x_4$; S_6 is the beginning switch AND S_5 is the ending switch OR S_6 is the ending switch AND S_5 is the beginning switch. Since S_6 is attached to S_1, the maximum end-to-end delay is: MAX END-TO-END DELAY 5-6 = MAX END-TO-END DELAY 6 + MAX END-TO-END DELAY 1-5.

STEP 7.

Place S_7 and connect to S_6; additional end-to-end delays = 6 = no of switches already in the network. Switches already in the network are; S_1, S_2, S_3, S_4, S_5 and S_6. S_7 is attached to S_6.

1st maximum end-to-end delay is $x_7 + x_6$. S_7 is the beginning switch AND S_6 is the ending switch OR S_7 is the ending switch AND S_6 is the beginning switch, the maximum end-to-end delay is: MAX. END-TO-END DELAY 6-7.

2nd maximum end-to-end delay is $x_7 + x_6 + x_1$; S_7 is the beginning switch AND S_1 is the ending switch OR S_7 is the ending switch AND S_1 is the beginning switch. Since S_7 is attached to S_6, the maximum end-to-end delay is: MAX END-TO-END DELAY 1-7 = MAX END-TO-END DELAY 7 + MAX END-TO-END DELAY 1-6.

3rd maximum end-to-end delay is $x_7 + x_6 + x_1 + x_2$; S_7 is the beginning switch AND S_2 is the ending switch OR S_7 is the ending switch AND S_2 is the beginning switch. Since S_7 is attached to S_6, the maximum end-to-end delay is: MAX END-TO-END DELAY 2-7 = MAX END-TO-END DELAY 7 + MAX END-TO-END DELAY 2-6.

4th maximum end-to-end delay is $x_7 + x_6 + x_1 + x_2 + x_3$; S_7 is the beginning switch AND S_3 is the ending switch OR S_7 is the ending switch AND S_3 is the beginning switch. Since S_7 is attached to S_6, the maximum end-to-end delay is: MAX END-TO-END DELAY 3-7 = MAX END-TO-END DELAY 7 + MAX END-TO-END DELAY 3-6.

5th maximum end-to-end delay is $x_7 + x_6 + x_1 + x_2 + x_4$; S_7 is the beginning switch AND S_4 is the ending switch OR S_7 is the ending switch AND S_4 is the beginning switch. Since S_7 is attached to S_6, the maximum end-to-end delay is: MAX END-TO-END DELAY 4-7 = MAX END-TO-END DELAY 7 + MAX END-TO-END DELAY 4-6.

6th maximum end-to-end delay is $x_7 + x_6 + x_1 + x_2 + x_5$; S_7 is the beginning switch AND S_5 is the ending switch OR S_7 is the ending switch AND S_5 is the beginning switch. Since S_7 is attached to S_6, the maximum end-to-end delay is: MAX END-TO-END DELAY 5-7 = MAX END-TO-END DELAY 7 + MAX END-TO-END DELAY 5-6.

STEP 8.

Place S_8 and connect to S_1; additional end-to-end delays = 7 = no of switches already in the network. Switches already in the network are: S_1, S_2, S_3, S_4, S_5, S_6 and S_7. S_8 is attached to S_1 1st maximum end-to-end delay is $x_8 + x_1$. S_8 is the beginning switch AND S_1 is the ending switch OR S_8 is the ending switch AND S_1 is the beginning switch, the maximum end-to-end delay is: MAX. END-TO-END DELAY 1-8.

2nd maximum end-to-end delay is $x_8 + x_1 + x_2$; S_8 is the beginning switch AND S_2 is the ending switch OR S_8 is the ending switch AND S_2 is the beginning switch. Since S_8 is attached to S_1, the maximum end-to-end delay is: MAX END-TO-END DELAY 2-8 = MAX END-TO-END DELAY 8 + MAX END-TO-END DELAY 2-1.

3rd maximum end-to-end delay is $x_8 + x_1 + x_2 + x_3$; S_8 is the beginning switch AND S_3 is the ending switch OR S_8 is the ending switch AND S_3 is the beginning switch. Since S_8 is attached to S_1, the maximum end-to-end delay is: MAX END-TO-END DELAY 3-8 = MAX END-TO-END DELAY 8 + MAX END-TO-END DELAY 3-1.

4th maximum end-to-end delay is $x_8 + x_1 + x_2 + x_4$; S_8 is the beginning switch AND S_4 is the ending switch OR S_8 is the ending switch AND S_4 is the beginning switch. Since S_8 is attached to S_1, the maximum end-to-end delay is: MAX END-TO-END DELAY 4-8 = MAX END-TO-END DELAY 8 + MAX END-TO-END DELAY 4-1.

5th maximum end-to-end delay is $x_8 + x_1 + x_2 + x_5$; S_8 is the beginning switch AND S_5 is the ending switch OR S_8 is the ending switch AND S_5 is the beginning switch. Since S_8 is attached to S_1, the maximum end-to-end delay is: MAX END-TO-END DELAY 5-8 = MAX END-TO-END DELAY 8 + MAX END-TO-END DELAY 5-1.

6th maximum end-to-end delay is $x_8 + x_1 + x_6$; S_8 is the beginning switch AND S_6 is the ending switch OR S_8 is the ending switch AND S_6 is the beginning switch. Since S_8 is attached to S_1, the maximum end-to-end delay is: MAX END-TO-END DELAY 6-8 = MAX END-TO-END DELAY 8 + MAX END-TO-END DELAY 6-1.

7th maximum end-to-end delay is $x_8 + x_1 + x_6 + x_7$; S_8 is the beginning switch AND S_7 is the ending switch OR S_8 is the ending switch AND S_7 is the beginning switch. Since S_8 is attached to S_1, the maximum end-to-end delay is: MAX END-TO-END DELAY 7-8 = MAX END-TO-END DELAY 8 + MAX END-TO-END DELAY 7-1.

4. The Upper-Delay Bounded Switched Local Area Network Design Algorithm

The upper-delay bounded switched LAN design algorithm is as follows:

Produce an undirected graph drawing of the network with the switches as the nodes (the hosts are excluded from the drawing).

Use the right-most pre-order transversal method to number the switches; S_i, i = 1, 2, 3,.. .,m, where m = the number of switches in the LAN.

Use the maximum delay model for an N-port switch to calculate the maximum end-to-end delay for switches S_i, i = 1, 2, 3, …,m.

maximum end-to-end delay for switch $1(S_1)$ = MAX END-TO-END DELAY 1

maximum end-to-end delay for switch $2(S_2)$ = MAX END-TO-END DELAY 2

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maximum end-to-end delay for switch $m(S_m)$ = MAX END-TO-END DELAY m

Placement of switches and computation of the end-to-end delays in the switched LAN.

Place switch $1(S_1)$

For i = 2, 3, 4, …,m, Do

Place switch i (S_i)

Assuming S_i is attached to S_r, and q switches have already been placed,

then there are:

q = i −1 additional maximum end-to-end delays;

the additional maximum end-to-end delays are given by:

MAX END-TO-END DELAY ri = $S_i + S_r$

MAX END-TO-END DELAY ji = $S_i + S_{jr}$; j = 1, 2, 3, …,q

$\neq r$

S_i = MAX END-TO-END DELAY i (maximum end-to-end delay for switch i)

S_r = MAX END-TO-END DELAY r (maximum end-to-end delay for switch r)

Sjr = MAX END-TO-END DELAY jr (maximum end-to-end delay of the switches on origin-destination path j-r)

Calculate the network average maximum end-to-end delay; NETWK AVE.MAX.END-TO-END DELAY

Calculate the network maximum of the maximum end-to-end delays; MAX-MAX END-TO-END DELAYS

Compare (e) or (f) with maximum delay requirements of the applications to be deployed in the network

If (e) or (f) is more than the maximum delay requirements of the application to be deployed in the network, upgrade switches and/or some inter-switch links to higher rates in order to make (e) or (f) to be less than the maximum delay requirements of the applications to be deployed in the network.

5. Conclusion

This paper has reported the development of an algorithm for designing upper-delay bounded switched LANs. The developed algorithm is part of a general research effort toward solving the slow response problem of many installed switched LANs. In a subsequent paper, we will report an example of the application of this algorithm to design a switched LAN.

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