A THREE PHASE ADAPTIVE ACTIVE LINE DETECTOR FOR SINGLE PHASE FED PREMISES[1,2]

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ABSTRACT:

The problem of increasing the power availability to single fed premise via automatic selection of an appropriate active phase of a three-phase feed line is addressed. Simulations were carried out on Control logic circuit power supply adequacy under scenarios of single and dual phase Mains failure. Design of hardware pertinent to the conditioning of each Mains phase line to the Control logic circuitry is presented. System performance characteristics under combinations of 'brown-outs' of the three line voltages is also presented.

INTRODUCTION

The majority of residential houses in developing countries are single phase fed. Characteristic of utility supply in developing countries is incessant brownouts or blackouts in one or more of the usual three- phase line feeds due to faulty line conditions [3]. Brownouts could be damaging to residential appliances and blackouts render the whole appliances in single phase fed residences inoperative. We present an innovative design that adaptively selects single line feed from the normal 4-wire 3-phase supply according to whether any one of the three phase Mains line voltage falls below a predefined datum voltage level hence unsuitable for feed into the single phase fed premise. The consequential effect is to increase the availability of immovable electrical appliances in single phase wired premises over those in three phase wired premises. The contrivance therefore makes single phase wiring an attractive proposition over the expensive installation and maintenance costs for three- phase wired building outlays. The utility provider also benefits since disconnection of a load from a brownout phase alleviates phase overload with consequential decrease in burnt distribution transformers.

DESIGN OVERVIEW

We use a weighted line prioritization approach to model feed line selection pivoted on phase one active contingency of a 4-wire, 3-phase power system.

In the modeling, phase one, tagged Φ1, is the phase the layout design Engineer would use to connect the single phase wired residence to the local distribution network in the absence of a three phase feed to the Controller. The other two phase lines tagged Φ2 and Φ3, provide redundancy and are automatically selected as per availability. Fig.1. illustrates a basic block schematic of the Adaptive Line Selector.

The design is split into three subunits.

(i) ***The Line Conditioning Sub-unit***

The unit is essentially a peak detector circuit incorporating zener diode over-voltage stabilization as well as voltage division circuitry [1,2,4,5] such that when the A.C. line voltage is 220V AC RMS (311V peak) its output is approximately 1.7V D.C. and clamped at 1.7V D.C. for A.C. line voltages greater than 220V RMS. The unregulated D.C. output voltage varies with A.C. peak line voltages less than 220V RMS. The lower TTL switching threshold of approximately 1.5V corresponds to A.C. line input voltage of 190V RMS (268V peak). Since the output of the line conditioning unit is used as trigger input to the logic sub-unit input gates, the configuration ensures a lower threshold of line 'good' of 190V RMS.

For design conceptualization, consider the generalized model of the line conditioning circuit of Fig.2.

The s-domain output voltage $v_i(s)$:

$$v_i(s) = \frac{v(s)R}{[R + R_d(1+sRC)]} \quad \text{.....(1)}$$

where V is the half-wave rectified input waveform to the filter section (Fig.2).

The Laplace transform for the half-wave rectified voltage, V, of period 2⊥ and amplitude V_m is related as [8]:

$$v(s) = V_m \frac{\pi\tau}{(\tau^2 s^2 + \pi^2)(1 - e^{-\tau s})} \quad \text{.....(2)}$$

Substituting (2) in (1) gives

$$v_i(s) = \frac{V_m \pi\tau R}{[R + R_d(1+sRC)](\tau^2 s^2 + \pi^2)(1 - e^{-\tau s})} \quad \text{.....(3)}$$

inverse Laplace transforming (3)[6] gives:

$$V_i(t) = \frac{\left[\tau R \sin\left(\frac{\pi}{\tau}\right)t + \tau R_d \sin\left(\frac{\pi}{\tau}t\right) - R_d RC\cos\left(\frac{\pi}{\tau}t\right)\pi + R_d RC\exp\left[\frac{-(R_d+R)}{(R_d RC)}t\right]\pi\right]}{\left[(R_d^2R^2C^2\pi^2 + \tau^2R^2 + 2\tau^2R_dR + \tau^2R_d^2)\pi\right]} V_m \pi\tau R$$

.....(4)

Expression (4) allows us to enumerate the voltage V_i, at the gate input at any arbitrary time, t; hence the voltage droop between two time intervals can be enumerated. It also indicates that cycle voltage peaks vary in magnitude with time, the exponential term causing a tailing off in cycle peak value variations as $t \to \infty$. The relation is thus most useful for design characterization of peak detectors. A practical circuit for the line conditioning circuit is given in Fig.3. Sample output characteristics are given in Fig.4. [7].

(ii) ***The D.C. Power supply Sub-unit***

The D.C. power supply sub-unit is required to provide steady D.C. power to the selector logic unit from a three-phase, 4-wire 220V A.C. Mains supply under failure of one or two of the Mains supply phases.

The classical 3-phase A.C. to D.C. converter, with slight modifications by the use of directional diodes, feeds a 5V D.C. regulator IC to provide D.C. power to the logic sub-unit. Hand calculation estimates of the behavior of the 3-phase converter follow similar steps as for the peak detector circuit. The A.C. supply voltage to the converter is provided by three 220V to 12V step-down transformer as illustrated in Fig.5. Power supply transient response simulations for rated load at the outputs of the converter and regulator (supply points A and B (Fig.5)) under full 3-phase Mains operation, single phase Mains failure, and two phase Mains failure are depicted in Fig.6. [7]. The transient responses show adequate Power supply D.C. voltage output stability at rated load under failure of one or two of the Mains phases.

(iii) ***The Selector Logic Sub-unit [1,2]***

Phase line selection is prioritized with respect of arbitrarily allocated order of phases- Phase 1 (ϕ1), Phase 2 (ϕ2), and Phase 3 (ϕ3). For the purposes of this paper, an active phase line is a line whose voltage value exceeds 190V RMS.

Phase line selection logic is:

(Phase 1 is selected if and only if Phase 1 is active)

while

(Phase 2 is selected if and only if ((Phase 2 is active) OR (Phase 2 and Phase 3 is active)) AND (Phase 1 is not active))

while

(Phase 3 is selected if and only if Phase 3 ALONE is active) .....(5)

Relation (5) prioritizes the selection such that when all three phase lines are active Phase 1 again would be selected for connection to the output (the premise). Phase 1 **must** therefore be the phase the layout design Engineer would normally connect the premise to in the absence of the controller.

If Phase 1 and Phase 2 lines are active, or Phase 1 and Phase 3 lines are active, priority is again given to Phase 1 for connection to the output.

If Phase2 alone is active, or Phase 2 and Phase 3 are active and Phase 1 is not active, priority is given to Phase 2 for output connection.

Phase 3 is selected if and only if it is the only active line.

If the line voltages on all the three phases fall below 190V, then none of the lines is selected to the output. The output load is therefore protected

from brownout voltages of less than 190V RMS under all situations.

The adaptive or prioritized switching swings into action under abnormal situations at the customer's distribution transformer end some of which may not be detectable at the local control center, as outlined by John Tweedy [3]. It does not disturb the utility provider's power layout scheme under normal operations of the phases.

The adaptive switching is an added bonus to the usual line load assignment since switching would only be effected to a line that is not overloaded.

Logical relation (5) can be subdivided into three parts for the purposes of Karnauph logic mapping.

The first part,) **(Phase 1 is selected if and only if Phase 1 is active** has mapping:

	ϕ_1	$\underline{\phi_1}$
$\underline{\phi_2}\ \underline{\phi_3}$	**1**	**0**
$\underline{\phi_2}\ \phi_3$	**1**	**0**
$\phi_2\ \underline{\phi_3}$	**1**	**0**
$\phi_2\ \phi_3$	**1**	**0**

We represent logical or level inversion with an underscore of the pertinent variable.

The table gives the output $Y1(\phi_1,\phi_2,\phi_3) = \phi_1$ (Fig.7).

The second part, **(Phase 2 is selected if and only if ((Phase 2 is active) OR (Phase 2 and Phase 3 is active)) AND (Phase 1 is not active))** has mapping:

	ϕ_1	$\underline{\phi_1}$
$\underline{\phi_2}\ \underline{\phi_3}$	**0**	**0**
$\underline{\phi_2}\ \phi_3$	**0**	**0**
$\phi_2\ \underline{\phi_3}$	**0**	**1**
$\phi_2\ \phi_3$	**0**	**1**

giving the output $Y2(\phi_1,\phi_2,\phi_3) = \underline{\phi_1}\ \phi_2$ (Fig.7).

The third part, **(Phase 3 is selected if and only if Phase 3 ALONE is active)** has mapping:

	ϕ_1	$\underline{\phi_1}$
$\underline{\phi_2}\ \underline{\phi_3}$	**0**	**0**
$\underline{\phi_2}\ \phi_3$	**0**	**1**
$\phi_2\ \underline{\phi_3}$	**0**	**0**
$\phi_2\ \phi_3$	**0**	**0**

giving the output $Y3(\phi_1,\phi_2,\phi_3) = \underline{\phi_1}\ \underline{\phi_2}\ \phi_3$.

The low voltage level signal activated PNP transistors are used as high current level relay drivers. This effectively reduces chip count (Fig.7).

The input-output state mapping of the three input phases, (ϕ_1, ϕ_2, ϕ_3) against the three logical output lines has representation:

	ϕ_1	$\underline{\phi_1}$
$\underline{\phi_2}$ $\underline{\phi_3}$	**Y1**	**0**
$\underline{\phi_2}$ ϕ_3	**Y1**	**Y3**
ϕ_2 $\underline{\phi_3}$	**Y1**	**Y2**
ϕ_2 ϕ_3	**Y1**	**Y2**

The three outputs are exclusive Ored together using transistor relay logic (Fig.7) to give the desired single selector output

$Y(\phi_1,\phi_2, \phi_3) = Y1(\phi_1,\phi_2, \phi_3) \oplus Y2(\phi_1,\phi_2, \phi_3) \oplus Y3(\phi_1,\phi_2,\phi_3)$.

Transient response of the single phase output $Y(\phi_1,\phi_2, \phi_3)$ for various scenarios of ϕ_1,ϕ_2, ϕ_3 are given in Fig.8 [7].

Note is taken, aside of the line phase delays, of the conspicuous delay introduced to responses at output Y (Fig.8) due to inherent delays introduced by the line conditioner circuitry responses (Fig.4) thus offering protection to output load from line transients.

CONCLUSIONS

For premises with low load demand, single-phase supply offers a lower installation cost in comparison to three-phase. However, the availability factor of single-phase supply to a premise is lower than that of three-phase supply in situations of line outages and brownouts due to line faults and line overloads.

It is demonstrated that the ingenious line selector design increases Mains availability to a single phase wired premise to the optimum possible without the risk of damaging line brownouts that could exist in a three-phase supplied premise. This implies that with the Selector, the power availability for a single phase wired premise is increased over that of the three-phase wired premise.

Delay incorporated in the design protects equipments in the premise against switch-on Mains supply voltage surges.

Selector logic operation is assured for all conditions of designed Mains operation.

For existing single-phase wired outlay, the ϕ_1 line is the existing line to the premise, hence the utility provider's layout is not disturbed under normal network operations.

No other changes to the outlay are required aside from extension of the remaining two of the three phase lines to the line selector. Installation simplicity with minimal overhead costs is therefore assured.

The utility service provider also benefits since automatic disconnection from a brownout line to another active line alleviates load stress on the brownout line with further consequential benefits to the power consumers.

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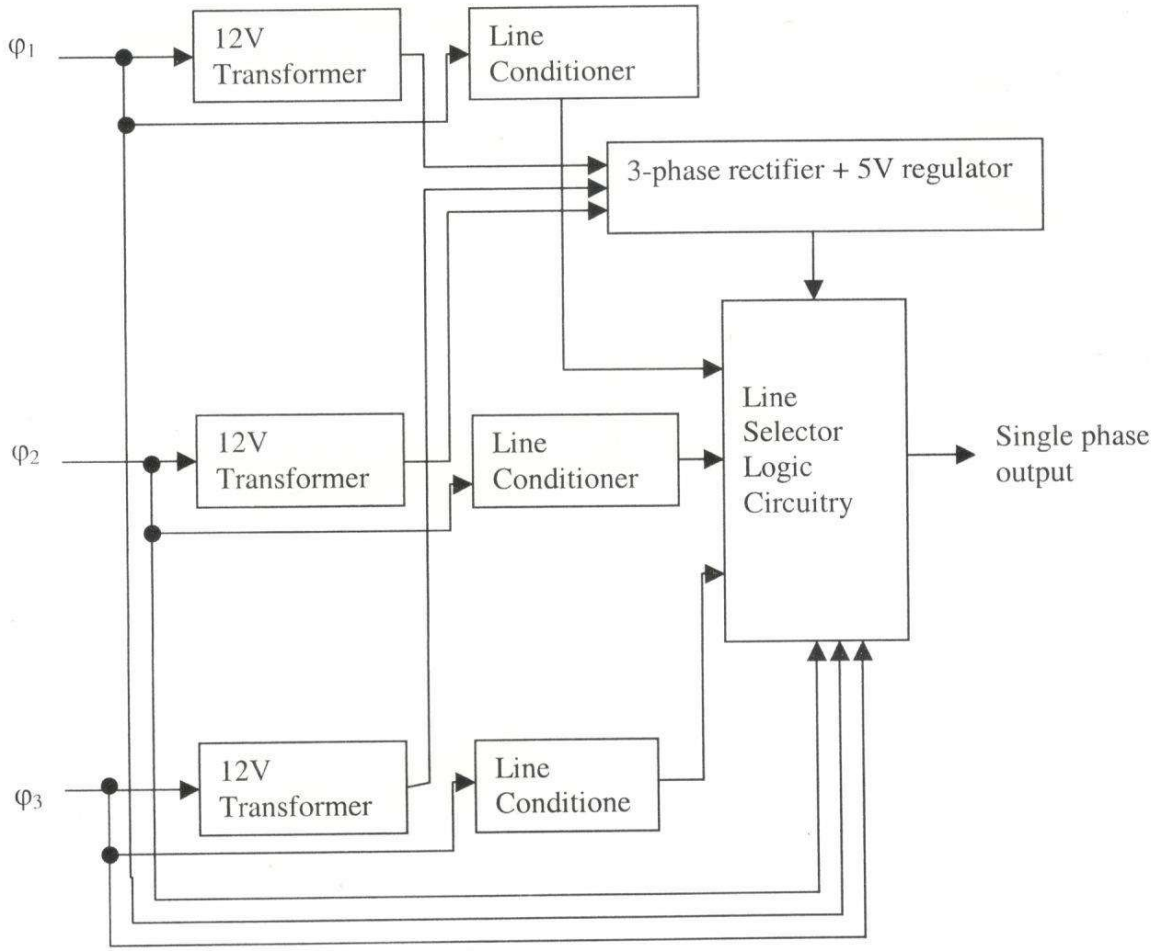

Fig.1: Block schematic of the Adaptive Line Selector

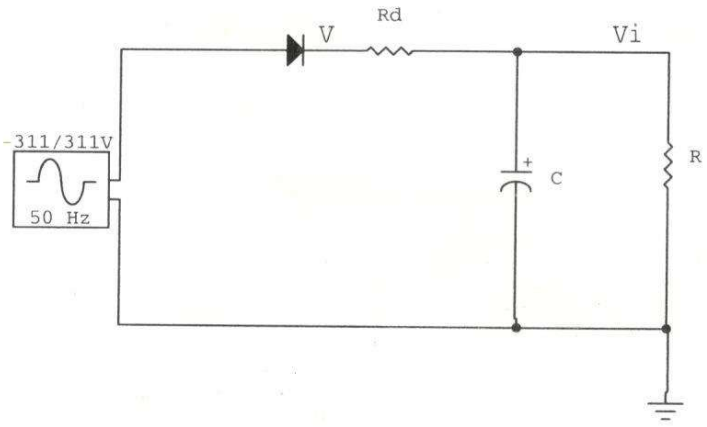

Fig. 2: A peak detector circuit

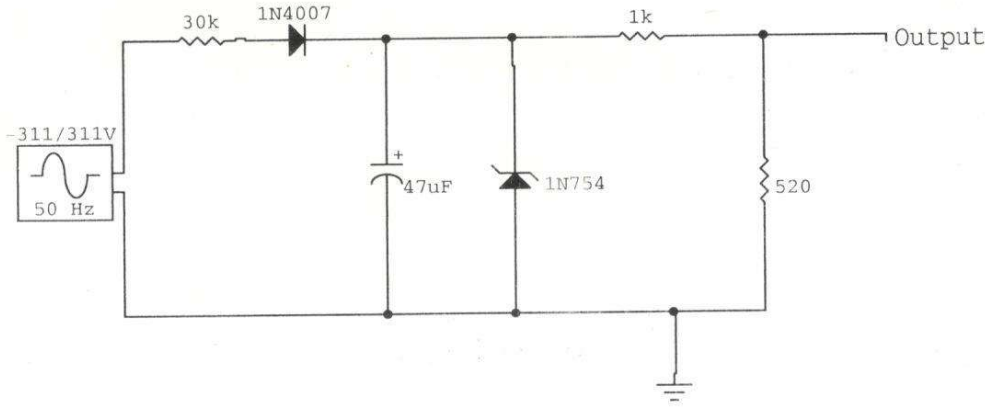

Fig.3. Circuit diagram of the line conditioner subunit

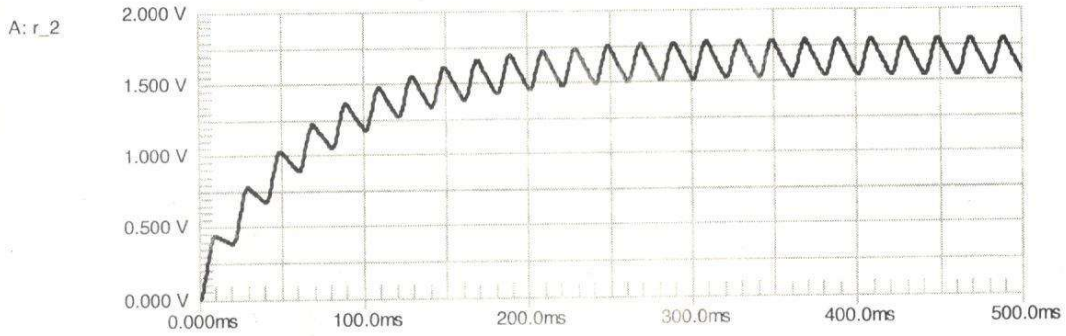

Fig.4.1: Line conditioner transient output response with Mains input voltage of 220V RMS

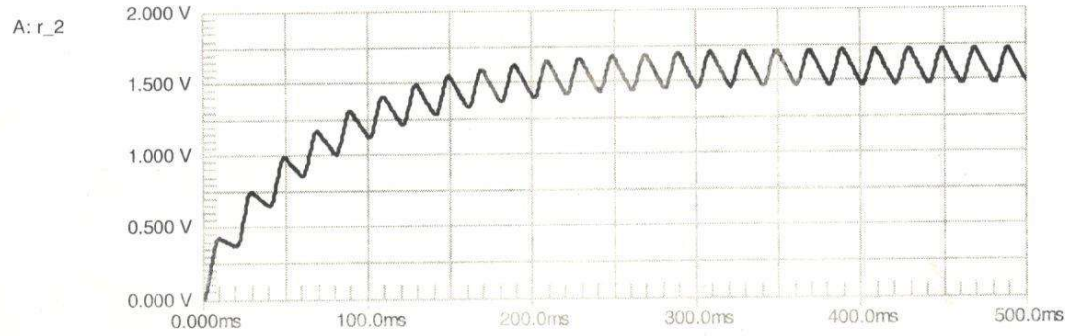

Fig.4.2: Line conditioner transient output response with Mains input voltage of 211V RMS

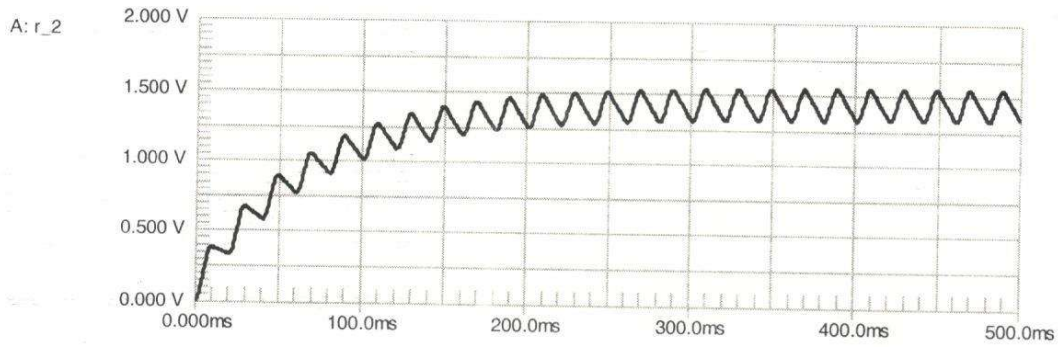

Fig.4.3: Line conditioner transient output response with Mains input voltage at marginal value of 190V RMS

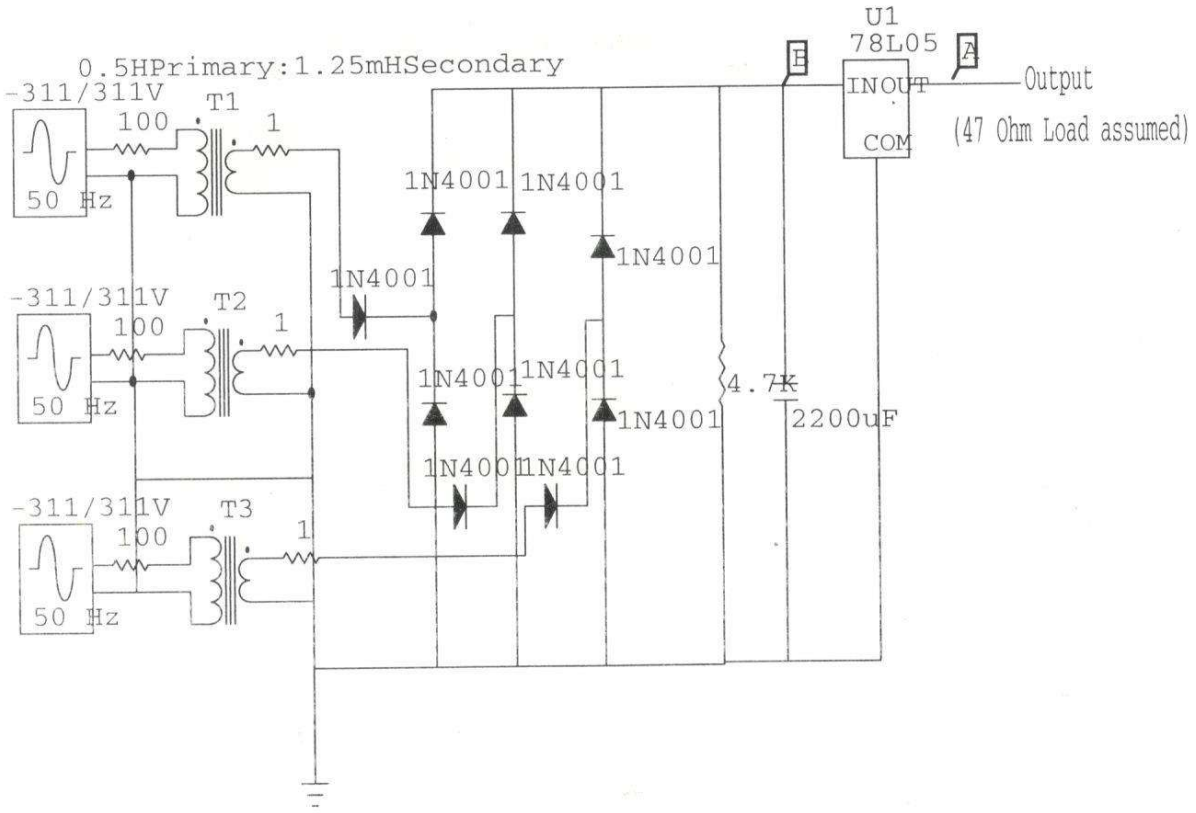

Fig 5. Schematic of Line selector power supply

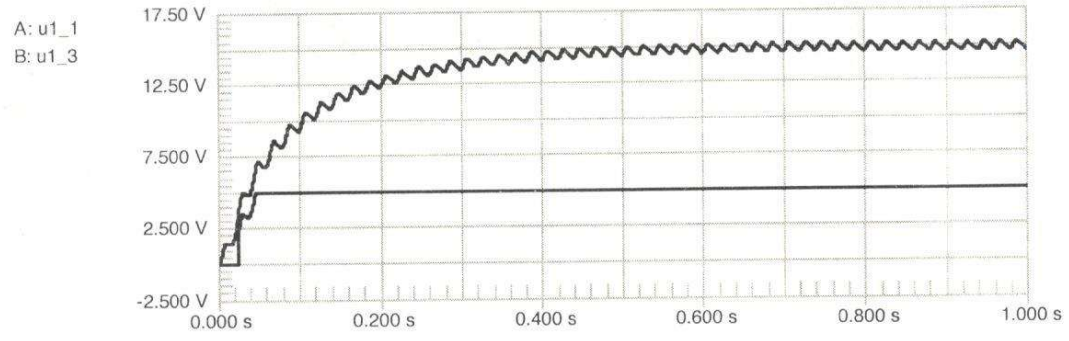

Fig.6.1: Transient outputs at points A and B (Fig.5) under full Mains operation

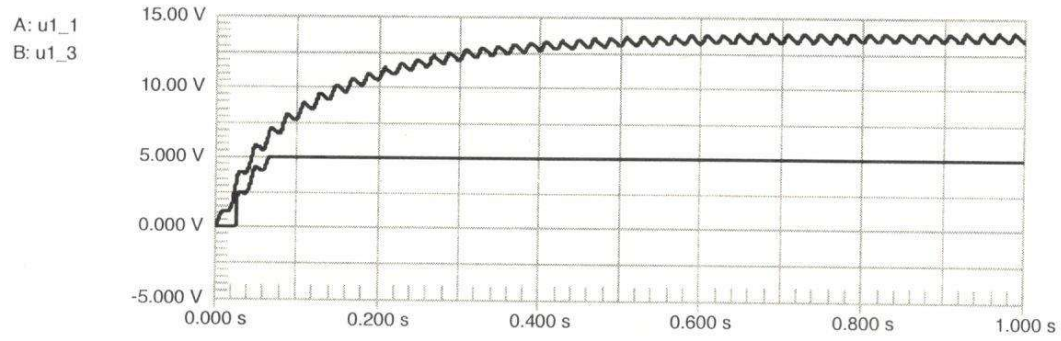

Fig.6.2: Transient outputs at points A and B (Fig.5) under two phase(ϕ_2, ϕ_3) Mains operation

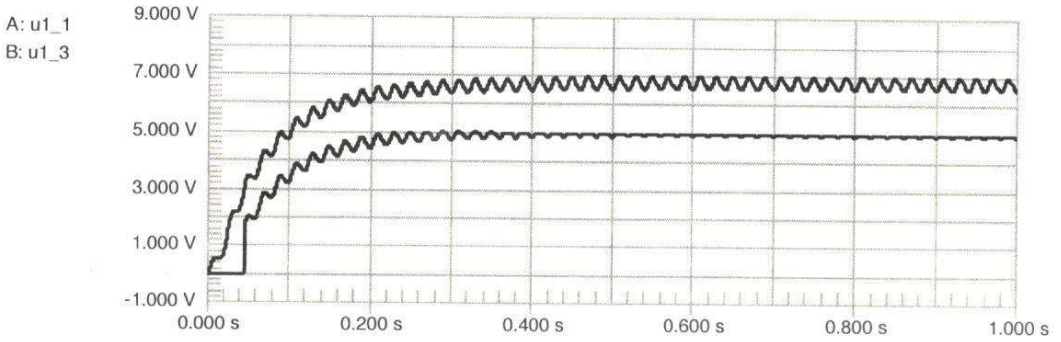

Fig.6.3: Transient outputs at points A and B (Fig.5) under single Phase (ϕ_3), Mains operation

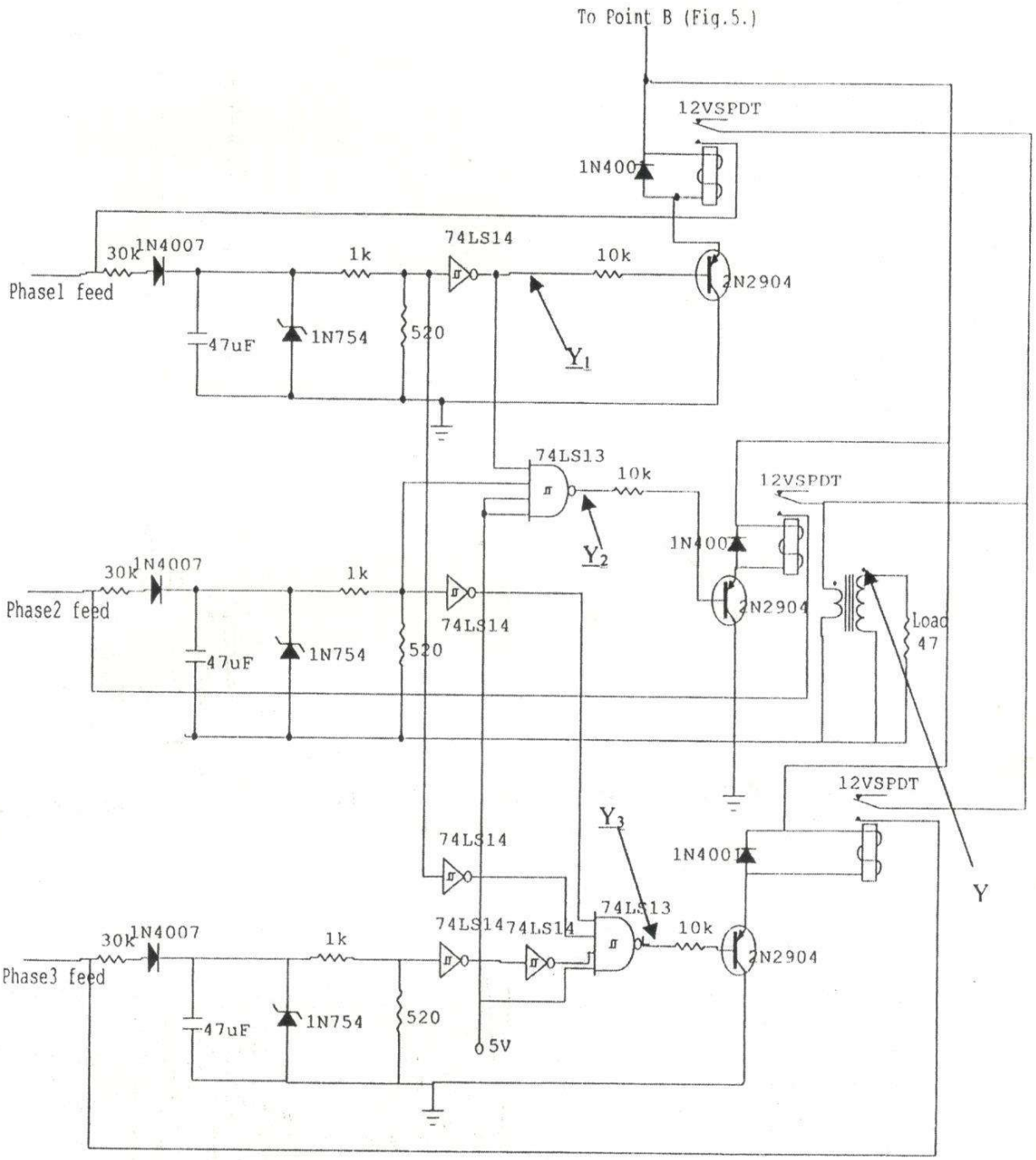

Fig.7, Schematic of the Selector Logic subunit incorporating Line conditioner subunit.

Transient response of the single phase output $Y(\phi_1,\phi_2,\phi_3)$ for various scenarios of ϕ_1,ϕ_2,ϕ_3 are given in Fig.8 [7]

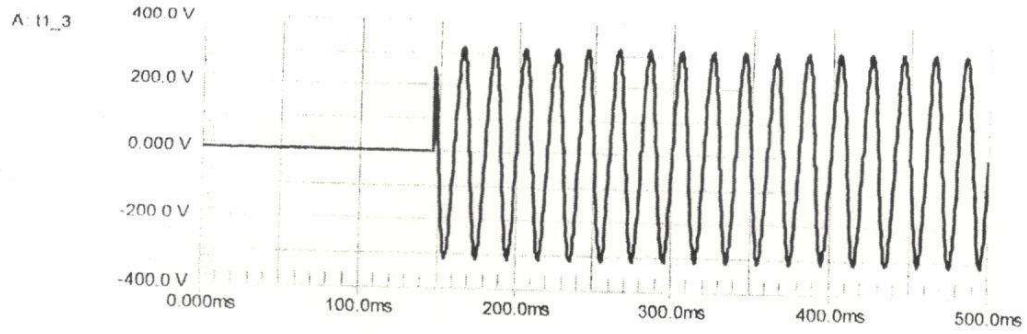

Fig.8.1. Transient response at output Y (Fig.7) with all lines active at 220VRMS.

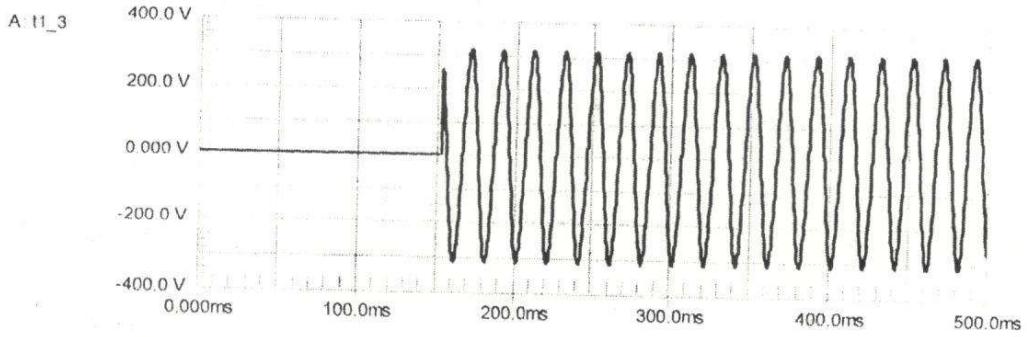

Fig.8.2. Transient response at output Y (Fig.7) with ϕ_1 inactive and ϕ_2, ϕ_3 active at 220VRMS.

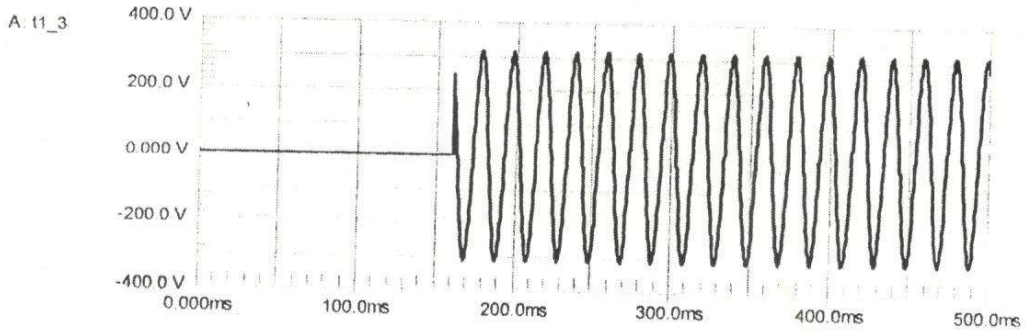

Fig.8.3. Transient response at output Y (Fig.7) with ϕ_1, ϕ_2 inactive and ϕ_3 active at 220VRMS.